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EXAMINER	
MANOSKEY, JOSEPH D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,210	SUH ET AL.	
	Examiner	Art Unit	
	JOSEPH D. MANOSKEY	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30,32,37-41,43,48-53 and 57* is/are rejected.

7)☒ Claim(s) *31,33-36,42,44-47,54-56 and 58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki (US 5,987,632) in view of Zagar et al (US 5,970,008).

3. As per claim 1, Irrinki discloses:

A semiconductor memory device comprising:

an array of memory cells arranged in rows and columns (column 2 lines 41-43: lines 57-59: columns. Figure 4 is an illustration);

means for selecting, for testing, the memory cells of the array in a repair unit in a test operation mode (Fig. 4, column 2 lines 20-29: rows and columns are each tested and evaluated individually);

means for measuring standby current of the memory cells selected for testing while in the test operation mode (column 9 lines 51- 62: tests may be performed on each row and column individually, including leakage tests, therefore standby current).

Irrinki does not disclose:

means for supplying a power voltage to the memory cells selected for testing in the test operation mode, and turning off power to remaining memory cells not selected for testing in the test operation mode;

means for restoring power voltage to memory cells no selected for testing, in a normal operation mode.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

4. As per claim 2, Irrinki and Zagar disclose:

The semiconductor memory device of claim 1, wherein the memory cells of the array are repaired in a row unit (See Irrinki, column 9 lines 9-17).

5. As per claim 3, Irrinki and Zagar disclose: The semiconductor memory device of claim 2, wherein the selection means selects the memory cells of the array in the repair unit in response to a row address in the test operation mode (See Irrinki, column 2 lines 41-49, 57-65).

6. As per claim 4, Irrinki and Zagar disclose: The semiconductor memory device of claim 2, wherein the power voltage supplying means comprises a fuse (See Irrinki, column 8 lines 10-23).

7. As per claim 5, Irrinki and Zagar disclose: The semiconductor memory device of claim 4, wherein in the test operation mode, whether or not the selected memory cells comprise a memory cell having standby current failure is judged depending on variation of the power voltage (See Irrinki, column 9 lines 51-53: the circuit is tested for leakage currents).

8. As per claim 6, Irrinki and Zagar disclose: The semiconductor memory device of claim 5, wherein the fuse of the power supplying means is cut when the selected memory cells comprise the memory cell causing the standby current failure (See Irrinki, column 9 lines 26-31, 34-38).

9. As per claim 7, Irrinki and Zagar disclose: The semiconductor memory device of claim 2, wherein the memory cells of the array are repaired in a column unit (See Irrinki, column 9 lines 9-17).

10. As per claim 8, Irrinki and Zagar disclose: The semiconductor memory device of claim 7, wherein the selection means selects the memory cells of the array in the repair unit in response to a column address in the test operation mode (See Irrinki, column 2 lines 41-49, 57-65).

11. As per claim 9, Irrinki and Zagar disclose: The semiconductor memory device of claim 8, wherein the power voltage supplying means comprises a fuse (See Irrinki, column 8 lines 10-23).

12. As per claim 10, Irrinki and Zagar disclose: The semiconductor memory device of claim 9, wherein in the test operation mode, whether or not the selected memory cells comprise the memory cell having the standby current failure is judged depending on variation of the power voltage (See Irrinki, column 9 lines 51-53: the circuit is tested for leakage currents).

13. As per claim 11, Irrinki and Zagar disclose: The semiconductor memory device of claim 10, wherein the fuse of the power voltage supplying means is cut when the

selected memory cells comprise the memory cell having the standby current failure (See Irrinki, column 9 lines 26-31, 34-38).

14. As per claim 50, Irrinki discloses:

A method for judging standby current failure in a semiconductor memory device having an array of memory cells arranged in rows and columns, the method comprising the steps of:

generating selection signals for selecting, for testing, the memory cells of the array in a repair unit during a test operation mode (column 2 lines 20-29: rows and columns are each tested and evaluated individually); and

measuring standby current of the memory cells selected for testing while in the test operation mode; and judging whether the selected memory cells comprise a memory cell having standby current failure, depending the measured standby current (column 9 lines 51- 62: tests may be performed on each row and column individually, including leakage tests, therefore standby current).

Irrinki does not disclose:

supplying a power voltage to the memory cells selected for testing in the test operation mode in response to the selection signals and turning off power-supply to the remaining memory cells not selected for testing in the test operation mode;

restoring power-supply to the remaining memory cells no selected for testing, in a normal operation mode.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

15. Claims 12-15, 18-21, 28, 32, 39, 43, 51, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki (US 5,987,632) in view of Zagar et al (US 5,970,008) and Hseih (US 5,710,550).

16. As per claim 12, Irrinki discloses:

A semiconductor memory device comprising:

a pad for receiving a power voltage (column 9 lines 26-31, 34-38: fuses can be blown to individual rows and columns, column 9 lines 51-62: voltage tests may be performed on each row and column);

a first power line connected to the pad (column 9 lines 26-31, 34-38: fuses can be blown to individual rows and columns, column 9 lines 51-62: voltage tests may be performed on each row and column);

an array of memory cells arranged in rows and columns (column 2 lines 41-43: lines 57-59: columns. Figure 4 is an illustration);

power lines connected to a corresponding repair unit (column 9 line 51 - column 10 line 3);

a selection circuit for outputting selection signals for selecting for testing the memory cells corresponding to one of the repair units in response to a row address in a test operation mode (column 2 lines 20-29: rows and columns are each tested and evaluated individually);

Irrinki does not disclose:

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns

a plurality of second power lines, each of the plurality of second power lines connected to a corresponding repair unit; and

a switch circuit operating in response to the selection signals, for connecting the second power line connected to the memory cells selected for testing with the first power line and disconnecting remaining second power lines from the first power line, in the test operation mode such that power is turned off from the memory cells not

selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

Hseih discloses a system which test a plurality of memory arrays connected together in a bus. The system is able to connect any one of the memory arrays on the bus individually (column 10 line 55 - column 11 line 8, and figure 5). Using this system would have the obvious benefit of being able to test multiple memory arrays, or work in an environment where more than one memory array is on a bus. Irrinki discloses that his system is designed to test memory arrays on a bus (column 8 lines 25-28), on an end user's system (column 2 lines 5-10). Using the multiple memory array system of Hseih would enable the memory testing system of Irrinki to test multiple memory arrays, or work an environment where more than one device is connected to the bus. Therefore, it would have been obvious to one of ordinary skill in the art at the time of

invention to incorporate multiple memory arrays into the memory system of Irrinki, increasing flexibility.

17. As per claim 13, Irrinki discloses:

The semiconductor memory device of claim 12, wherein the switch circuit comprises a fuse (column 8 lines 10-23).

18. As per claim 14, Irrinki discloses:

The semiconductor memory device of claim 13, wherein in the test operation mode, whether or not the selected memory cells comprise the memory cell having standby current failure is judged depending on variation of the power voltage (column 9 lines 51-53: the circuit is tested for leakage currents).

19. As per claim 15, Irrinki discloses:

The semiconductor memory device of claim 14, wherein the fuse of the switch circuit is cut when the selected memory cells comprise the memory cell having the standby current failure (column 9 lines 26-31,34-38).

20. As per claim 18, Irrinki discloses:

A semiconductor memory device comprising:

a pad for receiving a power voltage (column 9 lines 26-31, 34-38: fuses can be blown to individual rows and columns, column 9 lines 51-62: voltage tests may be performed on each row and column);

a first power line connected to the pad (column 9 lines 26-31, 34-38: fuses can be blown to individual rows and columns, column 9 lines 51-62: voltage tests may be performed on each row and column);

an array of memory cells arranged in rows and columns (column 2 lines 41-43: lines 57-59: columns. Figure 4 is an illustration);

power lines connected to a corresponding repair unit (column 9 line 51 - column 10 line 3);

a selection circuit for outputting selection signals for selecting for testing the memory cells corresponding to one of the repair units in response to a row address in a test operation mode (column 2 lines 20-29: rows and columns are each tested and evaluated individually); and

Irrinki does not disclose:

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns

a plurality of second power lines, each of the plurality of second power lines connected to a corresponding repair unit; and

a switch circuit operating in response to the selection signals, for connecting the second power line connected to the memory cells selected for testing with the first

power line and disconnecting remaining second power lines from the first power line, in the test operation mode such that power is turned off from the memory cells no selected for testing and in a normal mode, power is restored to the memory cells not selected for testing.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

Hseih discloses a system which test a plurality of memory arrays connected together in a bus. The system is able to connect any one of the memory arrays on the bus individually (column 10 line 55 - column 11 line 8, and figure 5). Using this system would have the obvious benefit of being able to test multiple memory arrays, or work in an environment where more than one memory array is on a bus. Irrinki discloses that his system is designed to test memory arrays on a bus (column 8 lines 25-28), on an end user's system (column 2 lines 5-10). Using the multiple memory array system of Hseih would enable the memory testing system of Irrinki to test multiple memory arrays,

or work an environment where more than one device is connected to the bus. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple memory arrays into the memory system of Irrinki, increasing flexibility.

21. As per claim 19, Irrinki discloses:

The semiconductor memory device of claim 18, wherein the switch circuit comprises a fuse (column 8 lines 10-23).

22. As per claim 20, Irrinki discloses:

The semiconductor memory device of claim 19, wherein in the test operation mode, whether or not the selected memory cells comprise the memory cell having standby current failure is judged depending on variation of the power voltage (column 9 lines 51-53: the circuit is tested for leakage currents).

23. As per claim 21, Irrinki discloses:

The semiconductor memory device of claim 20, wherein the fuse of the switch circuit is cut when the selected memory cells comprise the memory cell having the standby current failure (column 9 lines 26-31, 34-38).

24. As per claim 28, Irrinki discloses:

A semiconductor memory device comprising: a first power line for receiving a power voltage (column 9 line 51 - column 10 line 3: voltage tests are performed on the memory array based on different supply voltages); a repair unit comprising an array of memory cells arranged in rows and columns (column 2 lines 41-43: lines 57-59: columns. Figure 4 is an illustration);

a selection circuit for outputting selection signals for selecting for testing the rows in response to a row address (column 2 lines 20-29: rows and columns are each tested and evaluated individually);

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit (column 9 line 51 - column 10 line 3); and

Irrinki does not disclose:

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

outputting selection signals for selecting the rows in one of the repair units; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the rows of memory cells no selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be

operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

Hseih discloses a system which test a plurality of memory arrays connected together in a bus. The system is able to connect any one of the memory arrays on the bus individually (column 10 line 55 - column 11 line 8, and figure 5). Using this system would have the obvious benefit of being able to test multiple memory arrays, or work in an environment where more than one memory array is on a bus. Irrinki discloses that his system is designed to test memory arrays on a bus (column 8 lines 25-28), on an end user's system (column 2 lines 5-10). Using the multiple memory array system of Hseih would enable the memory testing system of Irrinki to test multiple memory arrays, or work an environment Where more than one device is connected to the bus. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple memory arrays into the memory system of Irrinki, increasing flexibility.

25. As per claim 32, Irrinki discloses:

The semiconductor memory device of claim 28, wherein the first power line is connected to a pad for receiving the power voltage (column 9 line 51 - column 10 line 3: voltage tests are performed on the memory array based on different supply voltages);

26. As per claim 39, Irrinki discloses:

A semiconductor memory device comprising:

a first power line for receiving a power voltage (column 9 line 51 - column 10 line 3: voltage tests are performed on the memory array based on different supply voltages);

a repair unit comprising an array of memory cells arranged in rows and columns (column 2 lines 41-43: lines 57-59: columns. Figure 4 is an illustration);

a selection circuit for outputting selection signals for selecting for testing the columns in response to a row address (column 2 lines 20-29: rows and columns are each tested and evaluated individually);

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit (column 9 line 51 - column 10 line 3);

Irrinki does not disclose:

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

outputting selection signals for selecting the rows in one of the repair units; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, and disconnecting the remaining second power

lines from the first power line, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

Hseih discloses a system which test a plurality of memory arrays connected together in a bus. The system is able to connect any one of the memory arrays on the bus individually (column 10 line 55 - column 11 line 8, and figure 5). Using this system would have the Obvious benefit of being able to test multiple memory arrays, or work in an environment where more than one memory array is on a bus. Irrinki discloses that his system is designed to test memory arrays on a bus (column 8 lines 25-28), on an end user's system (column 2 lines 5-10). Using the multiple memory array system of Hseih would enable the memory testing system of Irrinki to test multiple memory arrays, or work an environment where more than one device is connected to the bus.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple memory arrays into the memory system of Irrinki, increasing flexibility.

27. As per claim 43, Irrinki discloses:

The semiconductor memory device of claim 39, wherein the first power line is connected to a pad for receiving the power voltage (column 9 line 51 - column 10 line 3: voltage tests are performed on the memory array based on different supply voltages).

28. As per claim 51, Irrinki discloses:

A semiconductor memory device comprising:

a first power line for receiving a power voltage (column 9 line 51 - column 10 line 3: voltage tests are performed on the memory array based on different supply voltages);

a repair unit comprising an array of memory cells arranged in rows and columns (column 2 lines 41-43: lines 57-59: columns. Figure 4 is an illustration);

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit (column 9 line 51 -column 10 line 3);

Irrinki does not disclose:

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

outputting selection signals for selecting for testing one of the repair units; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the repair units of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

Hseih discloses a system which test a plurality of memory arrays connected together in a bus. The system is able to connect any one of the memory arrays on the bus individually (column 10 line 55 - column 11 line 8, and figure 5). Using this system would have the obvious benefit of being able to test multiple memory arrays, or work in an environment where more than one memory array is on a bus. Irrinki discloses that his system is designed to test memory arrays on a bus (column 8 lines 25-28), on an end user's system (column 2 lines 5-10). Using the multiple memory array system of Hseih would enable the memory testing system of Irrinki to test multiple memory arrays,

or work an environment where more than one device is connected to the bus. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple memory arrays into the memory system of Irrinki, increasing flexibility.

29. As per claim 57, Irrinki discloses:

The semiconductor memory device of claim 51, wherein in the test operation mode, whether the memory cells of the selected repair unit comprise the memory cell having standby current failure is judged depending on variation of the power voltage (column 9 lines 51-53: the circuit is tested for leakage currents).

30. Claims 16, 17, 22, 23, 37, 38, 48, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki (US 5,987,632)in view of Zagar et al (US 5,970,008) and Hseih (US 5,710,550), as applied above, and in further view of Petschauer (5,361,232).

31. As per claim 16, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 12, further comprising a precharge circuit for precharging the columns.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49).

Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

32. As per claim 17, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 16, wherein the precharge circuit is inactivated during the test operation mode.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49). Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of

Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

33. As per claim 22, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 18, further comprising a precharge circuit for precharging the columns.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49). Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

34. As per claim 23, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 22, wherein the precharge circuit is inactivated during the test operation mode.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49). Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

35. As per claim 37, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 28, further comprising a precharge circuit for precharging the columns.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses

that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49). Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

36. As per claim 38, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 37, wherein the precharge circuit is inactivated during the test operation mode.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49). Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using

Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

37. As per claim 48, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 39, further comprising a precharge circuit for precharging the columns.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49). Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary

skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

38. As per claim 49, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 48, wherein the precharge circuit is inactivated during the test operation mode.

Petschauer discloses a system which disables the precharge circuit when testing a digital memory system (column 1 line 63 - column 2 line 19). Petschauer discloses that this enables the tester to detect different types of faults that would not be detectable in other tests, such as temperature cycling and timing tests (column 1 lines 41-49). Irrinki discloses that a variety of tests are performed, including temperature cycling and timing tests (column 9 lines 55-63, column 10 lines 1-3), and that the purpose of this is to provide self-repair circuitry in an end-user's system (column 2 lines 5-10). Using Petschauer's system would enable the memory test to detect other types of errors that would not otherwise be detectable with Irrinki's system alone. Additionally, the use of Hseih's multiple memory array system would enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the precharge circuit into the memory testing system of Irrinki, Zagar and Hseih, improving test capabilities.

39. Claims 24-27, 29, 40, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki (US 5,987,632) in view of Zagar et al (US 5,970,008) and

Hseih (US 5,710,550), as applied above, and in further view of Rabindran (US 4,173,029).

40. As per claim 24, Irrinki discloses:

A semiconductor memory device comprising:

an array of memory cells arranged in rows and columns (column 2 lines 41-43: lines 57-59: columns. Figure 4 is an illustration);

a selection circuit for selecting for testing the memory cells of the array in a test operation mode (Fig. 4, column 2 lines 20-29: rows and columns are each tested and evaluated individually);

Irrinki does not disclose:

a plurality of repair units,

a plurality of third power lines, each of the plurality of third power lines electrically connected to a corresponding repair unit;

a selection circuit for selecting the memory cells of the array in one of the repair units in a test operation mode; and

Hseih discloses a system which test a plurality of memory arrays connected together in a bus. The system is able to connect any one of the memory arrays on the bus individually (column 10 line 55 - column 11 line 8, and figure 5). Using this system would have the obvious benefit of being able to test multiple memory arrays, or work in an environment where more than one memory array is on a bus. Irrinki discloses that

his system is designed to test memory arrays on a bus (column 8 lines 25-28), on an end user's system (column 2 lines 5-10). Using the multiple memory array system of Hseih would enable the memory testing system of Irrinki to test multiple memory arrays, or work an environment where more than one device is connected to the bus. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple memory arrays into the memory system of Irrinki, increasing flexibility.

Irrinki and Hseih do not disclose:

first and second pads for respectively receiving a power voltage;

a first power line electrically connected to the first pad;

a second power line electrically connected to the second pad; a first switch circuit for selectively connecting the first and second power lines in response to a test operation mode signal;

a second switch circuit for connecting the second power line to the third power line connected to the selected memory cells selected for testing and disconnecting the remaining third power lines from the second power line, in the test operation mode such that power is turned off from the memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing.

Zagar teaches independently electrically isolating circuitry and testing the subarrays of the memory arrays to independently. If the subarrays are found to be

operable, as opposed to inoperable, they are used during normal operation (See Col. 1, line 57 to Col. 2, line 1). It would have been obvious to combine to one of ordinary skill in the art at the time of the invention the memory array testing of Irrinki with the independent testing of subarrays of Zagar. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because if any subarrays are in operable the can been isolated from the rest to produce a smaller memory array without washing the entire wafer (See Zagar Col. 2, lines 1-21).

Rabindran discloses a switching system which is able to connect multiple power supplies to a circuit using a switching mechanism. The switches are connected to 2 different power supplies, one high and one low, and can switch between the levels according to an operating signal (column 2 line 61 - column 3 line 22). Irrinki discloses that his system tests the memory array at high and low voltages, to prove that the array will work in a wide range of operating conditions (column 9 lines 53-55, column 10 lines 1-3). Irrinki does not disclose whether the method used to change the voltage input includes one or two separate power sources, as it is not essential to the invention. Using Rabindran's system would enable the voltage to switch between high and low states as required by Irrinki. Additionally, simple voltage switching systems are very well known in the art and can be adapted to a wide variety of electrical systems. The use of Hseih's multiple memory array system would also enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the voltage switching

system of Rabindran into the testing systems of Hseih and Irrinki, enabling the system to vary voltage levels.

41. As per claim 25, Irrinki discloses:

The semiconductor memory device of claim 24, wherein the second switch circuit comprises a fuse (column 8 lines 10-23).

42. As per claim 26, Irrinki discloses:

The semiconductor memory device of claim 25, wherein in the test operation mode, whether the selected memory cells comprise the memory cell having standby current failure is judged depending on variation of the power voltage (column 9 lines 51-53: the circuit is tested for leakage currents).

43. As per claim 27, Irrinki discloses:

The semiconductor memory device of claim 26, wherein the fuse of the second switch circuit is cut when the selected memory cells comprise the memory cell having the standby current failure (column 9 lines 26-31, 34-38).

44. As per claim 29, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 28, further comprising first and second pads for respectively receiving the power voltage.

Rabindran discloses a switching system which is able to connect multiple power supplies to a circuit using a switching mechanism: The switches are connected to 2 different power supplies, one high and one low, and can switch between the levels according to an operating signal (column 2 line 61 - column 3 line 22). Irrinki discloses that his system tests the memory array at high and low voltages, to prove that the array will work in a wide range of operating conditions (column 9 lines 53-55, column 10 lines 1-3). Irrinki does not disclose whether the method used to change the voltage input includes one or two separate power sources, as it is not essential to the invention. Using Rabindran's system would enable the voltage to switch between high and low states as required by Irrinki. Additionally, simple voltage switching systems are very well known in the art and can be adapted to a wide variety of electrical systems. The use of Hseih's multiple memory array system would also enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the voltage switching system of Rabindran into the testing systems of Hseih, Zagar and Irrinki, enabling the system to vary voltage levels.

45. As per claim 40, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 39, further comprising first and second pads for respectively receiving the power voltage.

Rabindran discloses a switching system which is able to connect multiple power supplies to a circuit using a switching mechanism. The switches are connected to 2

different power supplies, one high and one low, and can switch between the levels according to an operating signal (column 2 line 61 - column 3 line 22). Irrinki discloses that his system tests the memory array at high and low voltages, to prove that the array will work in a wide range of operating conditions (column 9 lines 53-55, column 10 lines 1-3). Irrinki does not disclose whether the method used to change the voltage input includes one or two separate power sources, as it is not essential to the invention. Using Rabindran's system would enable the voltage to switch between high and low states as required by Irrinki. Additionally, simple voltage switching systems are very well known in the art and can be adapted to a wide variety of electrical systems. The use of Hseih's multiple memory array system would also enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the voltage switching system of Rabindran into the testing systems of Hseih, Zagar and Irrinki, enabling the system to vary voltage levels.

46. As per claim 52, Irrinki, Zagar and Hseih do not disclose:

The semiconductor memory device of claim 50, further comprising first and second pads for respectively receiving the power voltage.

Rabindran discloses a switching system which is able to connect multiple power supplies to a circuit using a switching mechanism. The switches are connected to 2 different power supplies, one high and one low, and can switch between the levels according to an operating signal (column 2 line 61 - column 3 line 22). Irrinki discloses

that his system tests the memory array at high and low voltages, to prove that the array will work in a wide range of operating conditions (column 9 lines 53-55, column 10 lines 1-3). Irrinki does not disclose whether the method used to change the voltage input includes one or two separate power sources, as it is not essential to the invention. Using Rabindran's system would enable the voltage to switch between high and low states as required by Irrinki. Additionally, simple voltage switching systems are very well known in the art and can be adapted to a wide variety of electrical systems. The use of Hseih's multiple memory array system would also enable the system to test multiple memory arrays, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the voltage switching system of Rabindran into the testing systems of Hseih, Zagar and Irrinki, enabling the system to vary voltage levels.

47. Claims 30, 41, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki (US 5,987,632) in view of Zagar et al (US 5,970,008), Hseih (US 5,710,550), and Rabindran (US 4,173,029), as applied above, and in further view of Microsoft Computer Dictionary (fifth edition).

48. As per claim 30, Rabindran discloses:

The semiconductor memory device of claim 29, wherein the first power line is directly connected to the second pad (Rabindran figure 1: power supply is directly connected to a power line)

Irrinki, Zagar, Hseih, and Rabindran do not disclose:

[the first power line] is connected to the first pad through a switch transistor.

Microsoft Computer Dictionary discloses that a transistor is a commonly used solid state device which can be used for switching applications. It is also disclosed that a transistor is a fundamental component of almost all modern electronics. It would therefore be obvious to use a transistor to as a switching element between the first and second power supplies, as it is the fundamental component of almost all modern electronics.

49. As per claim 41, Rabindran discloses:

The semiconductor memory device of claim 40, wherein the first power line is directly connected to the second pad (Rabindran figure 1: power supply is directly connected to a power line)

Irrinki, Zagar, Hseih, and Rabindran do not disclose:

[the first power line] is connected to the first pad through a switch transistor.

Microsoft Computer Dictionary discloses that a transistor is a commonly used solid state device which can be used for switching applications. It is also disclosed that a transistor is a fundamental component of almost all modern electronics. It would therefore be obvious to use a transistor to as a switching element between the first and

second power supplies, as it is the fundamental component of almost all modern electronics.

50. As per claim 53, Rabindran discloses:

The semiconductor memory device of claim 52, wherein the first power line is directly connected to the second pad (Rabindran figure 1: power supply is directly connected to a power line)

Irrinki, Zagar, Hseih, and Rabindran do not disclose:

[the first power line] is connected to the first pad through a switch transistor. Microsoft Computer Dictionary discloses that a transistor is a commonly used solid state device which can be used for switching applications. It is also disclosed that a transistor is a fundamental component of almost all modern electronics. It would therefore be obvious to use a transistor to as a switching element between the first and second power supplies, as it is the fundamental component of almost all modern electronics.

Allowable Matter

51. Claims 31, 33-36, 42, 44-47, 54-56, and 58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

52. Applicant's arguments, see pages 17-19 of amendment, filed 26 June 2008, with respect to the rejection(s) of claim(s) 1-30,32,37-41,43,48-53 and 57 under 25 U.S.C. 102(b) and 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of new found prior art, see above rejection.

Conclusion

53. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH D. MANOSKEY whose telephone number is (571)272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
October 10, 2008

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113